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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,327	07/30/2003	Eitan Rosen	MP0280	1395
26200	7590	04/20/2007	EXAMINER	
FISH & RICHARDSON P.C. P.O BOX 1022 MINNEAPOLIS, MN 55440-1022			CHEN, TSE W	
		ART UNIT	PAPER NUMBER	
		2116		
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	04/20/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

ED

Office Action Summary	Application No.	Applicant(s)	
	10/631,327	ROSEN, EITAN	
	Examiner Tse Chen	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 26 March 2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-15 and 23-37 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-15 and 23-37 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 26 March 2007 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5-6, 11-14, 23-25, 27-28, 33-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Anzai, US Patent 6898722.

3. In re claims 1 and 23, Anzai discloses a circuit [fig.1], comprising associated means of:

- A clock transmitter [within 100] in communication with a clock bus [c], the clock transmitter to transmit a clock signal on the clock bus [fig.2c].
- A clock receiver [within 200] in communication with the clock bus, the clock receiver to receive a clock signal on the clock bus [col.5, ll.33-43].
- A driver [109] in communication with the clock bus, the driver to drive and maintain a voltage [e.g., low after completion signal] of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus [col.5, ll.52-65; col.6, ll.28-38; fig.5, transfer clock (L)].

4. As to claims 3 and 25, Anzai discloses, wherein the driver includes a resistance [inherently, circuitries comprise resistance in order to function properly].

5. As to claims 5 and 27, Anzai discloses, wherein the driver includes a transistor [col.1, ll.15-21; integrated circuitry].

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6. As to claims 6 and 28, Anzai discloses, including enabling circuitry [108] in communication with the driver, the enabling circuitry to enable the driver [i=5 drives j high] when the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus [col.7, ll.18-35].

7. As to claims 11 and 33, Anzai discloses, wherein the drive is included in a packet processor [fig.3] [col.6, ll.18-27; processing odd/even data packets].

8. As to claims 12 and 34, Anzai discloses, wherein the driver is included in a packet processor configured to transmit data and to receive data according to a double data rate protocol [col.5, ll.44-51].

9. As to claims 13 and 35, Anzai discloses, including a memory [103 and 207 constitutes a memory].

10. As to claims 14 and 36, Anzai discloses, wherein the memory is configured to transmit data and to receive data according to the double data rate protocol [col.5, ll.44-51].

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 2 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anzai.

13. Anzai discloses a circuit [fig.1], comprising associated means of:

- A clock transmitter [within 100] in communication with a clock bus [c], the clock transmitter to transmit a clock signal on the clock bus [fig.2c].

- A clock receiver [within 200] in communication with the clock bus, the clock receiver to receive a clock signal on the clock bus [col.5, ll.33-43].
 - A driver [109] in communication with the clock bus, the driver to drive a voltage [e.g., high] of the clock bus to a first voltage level [associated with completion signal] while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus [col.5, ll.52-65; col.6, ll.28-38; drives bus to high indicating clock transmission is complete].
 - Wherein the first voltage level is a voltage level corresponding to a logical one [high] [col.5, ll.52-65].
14. Anzai did not disclose explicitly continuing the data transmission.
15. Examiner had taken Official Notice that it is well known in the art to continue data transmission. It would have been obvious to one of ordinary skill in the art, having the teachings of Anzai before him at the time the invention was made, to continue data transmission after a data completion signal, resulting in the driver to drive and maintain a voltage [e.g., high] of the clock bus to a first voltage level [associated with completion signal] while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus, until the start of the next data sequence that occurs right after the data completion signal. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to transmit more data efficiently [i.e., no pause].
16. Claims 4 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anzai as applied to claims 3 and 25 above, and further in view of Masuda et al., US Patent 5732249, hereinafter Masuda.

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17. Anzai taught each and every limitation of the claim as discussed above. Anzai did not discuss details of the driver.

18. Masuda discloses a driver [fig.1] that includes a first resistance [r1] between the clock bus [1] and a voltage Vdd, and wherein the driver further includes a second resistance [r2] between the clock bus and ground.

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Anzai and Masuda before him at the time the invention was made, to modify the circuit taught by Anzai to include the driver explicitly taught by Masuda, in order to obtain the claimed circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to control clock skew [Masuda: abstract].

20. Claims 7 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anzai as applied to claims 6 and 28 above, and further in view of McDaniel et al., US Patent 5355468, hereinafter McDaniel.

21. Anzai taught each and every limitation of the claim as discussed above. Anzai did not disclose disabling the driver when the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

22. McDaniel discloses the enabling circuitry to disable the driver when the [clock] transmitter is not transmitting a [clock] signal on the [clock] bus and the [clock] receiver is not receiving a [clock] signal on the [clock] bus [col.11, ll.3-62; col.26, ll.7-11; disable when clock/data signal is not present].

23. It would have been obvious to one of ordinary skill in the art, having the teachings of Anzai and McDaniel before him at the time the invention was made, to modify the circuit taught

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by Anzai to include the teachings of McDaniel, in order to obtain the claimed circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to conserve power [McDaniel: col.26, ll.7-11].

24. Claims 8-10 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anzai as applied to claims 6 and 28 above, and further in view of Jeppesen III et al., US Patent 5355468, hereinafter Jeppesen.

25. Anzai taught each and every limitation of the claim as discussed above. Anzai did not disclose the receive processing clock to turn off in response to a signal from the enabling circuitry.

26. In re claims 8 and 30, Jeppesen discloses receive processing circuitry in communication with the enabling circuitry, the receive processing circuitry including a receive processing clock, the receive processing clock to turn off in response to a signal from the enabling circuitry [col.8, ll.3-6].

27. In re claims 9 and 31, Jeppesen discloses, wherein the enabling circuitry includes a flip flop [37].

28. In re claims 10 and 32, Jeppesen discloses, wherein the enabling circuitry enables the driver when the flip flop is in a first state [clip = high], and wherein the enabling circuitry disables the driver when the flip flop is in a second state [clip = low] [col.6, ll.11-19].

29. It would have been obvious to one of ordinary skill in the art, having the teachings of Anzai and Jeppesen before him at the time the invention was made, to modify the circuit taught by Anzai to include the teachings of Jeppesen, in order to obtain the receive processing clock that turns off in response to a signal from the enabling circuitry and the associated circuits. One

of ordinary skill in the art would have been motivated to make such a combination as it provides a predictable and accurate way to control timing [Jeppesen: col.2, ll.6-9].

30. Claims 15 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anzai as applied to claims 13 and 35 above.

31. Anzai taught each and every limitation of the claim as discussed above. Anzai discloses another clock receiver [e.g., b] associated with the clock transmitter and driver [fig.6]. Anzai did not disclose explicitly that the clock transmitter and driver are to be “another” separate entity. Examiner had taken Official Notice that it is well known in the art to use another entity [i.e., additional clock transmitter and driver] for fault tolerant redundancy.

32. It would have been obvious to one of ordinary skill in the art, having the teachings of Anzai before him at the time the invention was made, to modify the circuit taught by Anzai to include additional clock transmitter and driver, in order to obtain the claimed circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides fault tolerant redundancy against single point failures.

Response to Arguments

33. Applicant's arguments filed March 26, 2007 have been fully considered but they are not persuasive.

34. Applicant argues that Anzai fails to teach “a driver to drive and maintain a voltage of the clock bus to a first voltage level *while* the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus”. Examiner submits that the claim does not indicate when the maintaining of the voltage of the clock bus to a first voltage level begins. The claim indicates the maintaining of the voltage of the clock bus in

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reference to a first voltage level. In this case, the first voltage level shown as transfer clock (L) of fig.5 is set at low [first] voltage level after the completion signal [i.e., associated with completion signal] **while** the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

35. All other claims were not argued separately.

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

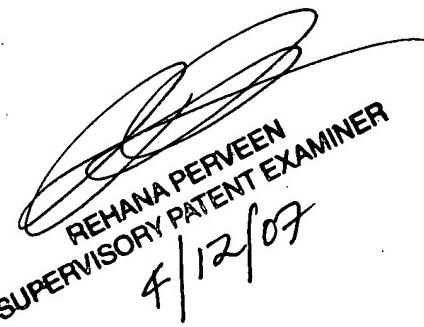
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
April 11, 2007



REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
4/12/07